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05SCS/05SCE11

First Semester M.Tech. Degree Examination, Dec 08 / Jan 09
Computer Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Differentiate between multiprocessors and multicomputers. Discuss the different models of multi processor systems giving the advantages and disadvantages of each. **(08 Marks)**

b. With the help of a neat diagram, explain the basic architecture of a vector processor. **(08 Marks)**

c. How are the various bounds specified using VLSI complexity model for parallel computers? **(04 Marks)**

2 a. Consider a processor which takes the following timing (in microseconds) for the different tasks as shown. Fetch : 0.1 ; decode : 0.25 ; execute : 1.5 and write back : 0.2. What is the speed up if this processor is pipelined (synchronous) with four stages as above for executing a program consisting of 1000 instructions? Also calculate the MIPS for each case while executing the above program. **(10 Marks)**

b. With the help of a neat diagram, explain the pipelined floating point adder. **(10 Marks)**

3 a. The forbidden latencies for a five stage non – linear pipelined processor is given by F = {5, 4, 3}. Draw the state transition diagram and determine the following :
i) Simple cycles and greedy cycles ii) Constants cycles iii) Minimum average latency (MAL) iv) Maximum through puts if the clock time T = 20nS. **(12 Marks)**

b. Explain how the Reorder Buffer (ROB) is implemented for maintaining sequential consistency. **(08 Marks)**

4 a. What are the operand fetch policies in the superscalar processor using shelved issue? Explain how the availability of operands are checked in each case. **(10 Marks)**

b. Explain how a CISC processor is implemented using superscalar RISC processor. **(10 Marks)**

5 a. With the help of suitable examples, explain the cache coherence problem. **(08 Marks)**

b. Explain the directory based protocol for cache coherence. **(12 Marks)**

6 a. What are the various design issues for the SIMD systems? Explain. **(10 Marks)**

b. Discuss the salient features of Cray C 90 systems. **(10 Marks)**

7 a. What are the important parameters considered in the design of interconnection networks? Explain. **(08 Marks)**

b. Design an 8× 8 Omega network and show the switch settings for the permutation $\pi = (0, 5, 4, 2)\ (1, 3)\ (4)$. Mark the switches which cause conflicts, if any. **(12 Marks)**

8 Write short notes on any TWO:
a. Systolic Architecture
b. Data flow Architecture
c. VLIW Architecture. **(20 Marks)**

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